HDAWG Specification

Arbitrary Waveform Generator	
channels	4 (HDAWG4 model) 8 (HDAWG8 model)
vertical resolution	16 bit
waveform memory per channel	64 MSa; 500 MSa (with HDAWG-ME option)
sequence memory	16384 instructions
waveform granularity	8 samples
minimum waveform length	32 samples
sequencer clock frequency	sampling rate divided by 8
sequencer instructions (playback)	play waveform (single or multi-channel), play waveform segment (start sample index and segment length), play waveform from the library (DIO input state), interrupt waveform playback
sequencer instructions (other)	wait constant, wait for trigger, set/get trigger state, set/get DIO state, integer variable operations (add, subtract, logical operations), change oscillator frequency/phase (real-time), change other instrument setting (non real-time)
sequencer control structures	repeat (1 to 2^{23}-1 or infinite), conditional branch (multi-branch)
Wave Output	
connector type	SMA
output impedance	50 Ω
output coupling	DC
output modes	amplified, direct
output range (into 50 Ω)	0.2 to 5.0 V_{pp} (amplified) 0.8 V_{pp} (direct)
offset voltage (into 50 Ω)	0.5 × peak voltage, max. ±1.25 V (amplified) 0 V (direct)
phase noise	<−110 dBc/Hz (100 MHz, offset 10 kHz)
voltage noise	30 nV/√Hz (amplified, 5 V_{pp} range)
above 200 kHz	12 nV/√Hz (direct)
Time & Frequency Domain Characteristics	
frequency range, max. amplitude	0 − 300 MHz, 5.0 V_{pp}
into 50 Ω	0 − 750 MHz, 0.8 V_{pp}
sampling clock source	internal, external
sampling rate	1.5 kSa/s to 2.4 GSa/s (internal clock) 50 MSa/s to 2.4 GSa/s (external clock)
internal sampling clock resolution	7 digits
rise time (20% to 80%)	< 550 ps (amplified, 1 V step, 5 V_{pp} output range) < 300 ps (direct, 0.8 V step)
trigger delay to output	< 50 ns
skew between channels	< 200 ps (any two channels) < 20 ps (channels 1&2, 3&4, ...)
skew adjustment range	10 ns
skew adjustment resolution	10 ps
Marker & Other Outputs	
marker outputs	2 per channel, 1 SMA output per channel on front panel, additional outputs on DIO on back panel
sampling clock output	SMA on back panel
sampling clock output amplitude	2 V_{pp}
reference clock output	SMA on back panel
reference clock output amplitude	1 V_{pp}
reference clock output frequency	10 / 100 MHz
Inputs	
trigger inputs	1 per channel, SMA on front panel
trigger input impedance	50 Ω / 1 kΩ
trigger input amplitude range	±5 V (50 Ω) ±10 V (1 kΩ)
trigger input threshold range	±5 V (50 Ω) ±10 V (1 kΩ)
trigger input threshold resolution	< 0.4 mV
sampling clock input	SMA on back panel

reference clock input	SMA on back panel
reference clock input frequency	10 / 100 MHz

Maximum Ratings

damage threshold Sampling Clock input	±5 V
damage threshold Ref input	±5 V

Connectivity & Others

digital IO (DIO)	VHDCI 68 pin female connector, 32 bit, configurable as input or output, 3.3 V TTL
host connection	LAN / Ethernet, 1 Gbit/s USB 3.0, 5 Gbit/s
PC memory requirements	4 GB+
PC CPU requirements	Compatibility with SSE2 instruction set required. Examples: AMD K8 (Athlon 64, Sempron 64, Turion 64, etc.), AMD Phenom, Intel Pentium 4, Xeon, Celeron, Celeron D, Pentium M, Celeron M, Core, Core 2, Core i5, Core i7, Core i3, Atom
operating system	See LabOne Compatibility

General

dimensions	43.0 × 23.2 × 10.2 cm 16.9 × 9.2 × 4.0 inch, suited for 19 inch rack
weight	4.6 kg; 10.2 lbs
power supply AC line	100-240 V (±10%), 50/60 Hz
operating temperature	+5 °C to +40 °C
operating environment	IEC61010, indoor location, installation category II, pollution degree 2
operating altitude	up to 2000 meters